C L A I M S

1. A circuit for demodulating at least one modulated signal such as a measuring signal of a sensor, comprising

at least one input to which the modulated signal may be applied, and

at least one switched-capacitor network connected to the input for demodulating the signal.

2. The circuit of claim 1, wherein the switched-capacitor network includes at least two inputs (e_{pos}, e_{neg}) and/or at least one switched-capacitor amplifier (5, 7, 9, 10, 11) and/or at least one switched-capacitor integrator (6, 8).

3. The circuit of claim 2, wherein the one switched-capacitor integrator comprises a negative, undelayed switched-capacitor integrator, and/or has an amplification of one.

4. The circuit of claim 2 wherein a first switched-capacitor amplifier (5) comprises a positive delayed switched-capacitor amplifier, and/or multiplies two input signals each by at least one factor (γ_1, γ_2).

5. The circuit of claim 4, wherein a second switched-capacitor amplifier (7) comprises a positive delayed switched-capacitor amplifier, and/or delays the applied input signal by a half cycle of a clock frequency, and/or has an amplification of one.

6. The circuit of claim 5, wherein a third switched-capacitor amplifier (9) comprises a positive

delayed switched-capacitor amplifier, and/or delays the applied input signal unamplified by a half cycle of the clock frequency.

7. The circuit of claim 6, wherein a fourth switched-capacitor amplifier (10) comprises positive delayed switched-capacitor amplifier, and/or delays the applied input signal unamplified by a half cycle of the clock frequency.

8. The circuit of claim 7, wherein a fifth switched-capacitor amplifier (11) comprises a positive delayed switched-capacitor amplifier, and/or delays the applied input signal unamplified by a half cycle of the clock frequency.

9. The circuit of claim 2, wherein the output of a first switched-capacitor amplifier (5) is applied to an input of the one switched-capacitor integrator (6, 8).

10. The circuit of claim 9, wherein the output of the switched-capacitor integrator (6, 8) is applied to a second input of the first switched-capacitor amplifier (5).

11. The circuit of claim 6 wherein the output of the second switched-capacitor amplifier (7) is applied to an input of the third switched-capacitor amplifier (9).

12. The circuit of claim 7, wherein the output of the third switched-capacitor amplifier (9) is applied to an input of the fourth switched-capacitor amplifier (10).

13. The circuit of claim 8, wherein the output of the fourth switched-capacitor amplifier (10) is applied to an input of the fifth switched-capacitor amplifier (11).

14. The circuit of claim 8, wherein the output of the fifth switched-capacitor amplifier (11) is applied to a second input of the switched-capacitor integrator (6, 8).

15. The circuit of claim 14, wherein the signal is applied to a third input of the switched-capacitor integrator (6, 8).

16. The circuit of claim 14 wherein the switched-capacitor integrator (8) includes at least two integrator capacitances.

17. The circuit of claim 16, wherein the two integrator capacitances are used, for storing a previous signal and/or computing the reflected voltage wave.

18. The circuit of claim 2, wherein the switched-capacitor network comprises a filter arrangement.

19. The circuit of claim 18, wherein the filter arrangement comprises an n-path lag wave filter that is formed by at least one of the switched-capacitor amplifiers (5, 7, 9, 10, 11) and/or the switched-capacitor integrator (6, 8).

20. The circuit of claim 18 wherein the coefficients of the filter arrangement are digitally programmable by means of at least one switch.

21. The circuit of one of claim 1 further comprising a further switched-capacitor network whereby the demodulated signal of positive and negative values of a carrier frequency can be added.

22. A method of demodulating a modulated measuring signal of a sensor comprising the steps of

applying the signal to an input of a switched-capacitor network and operating the network so as to demodulate the signal.

23. The method of claim 22, wherein the signal is filtered by means of a filter arrangement.

24. The method of claim 22, wherein the signal is converted to a square-wave signal.

25. The method of claim 22, wherein the signal is sampled at least once.

26. The method of claim 22, comprising the further step of adding positive and negative values of a carrier frequency of the demodulated signal by means of a further switched-capacitor network.